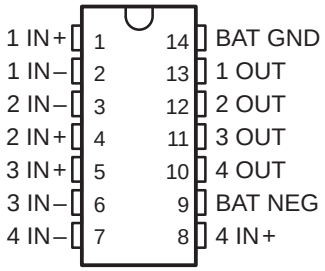
- **Designed for –52-V Battery Operation**
- **50-mA Output Current Capability**
- **Input Compatible With TTL and CMOS**
- **High Common-Mode Input Voltage Range**
- **Very Low Input Current**
- **Fail-Safe Disconnect Feature**
- **Built-in Output Clamp Diode**
- **Direct Replacement for National DS3680 and Fairchild μA3680**

D OR N PACKAGE
(TOP VIEW)

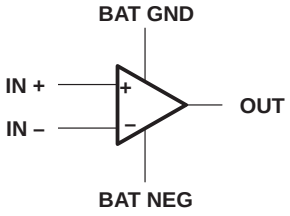


description

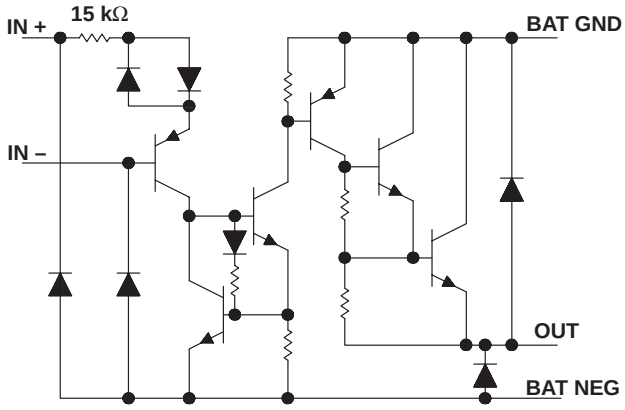
The DS3680 telephone relay driver is a monolithic integrated circuit designed to interface –48-V relay systems to TTL or other systems in telephone applications. It is capable of sourcing up to 50 mA from standard –52-V battery power. To reduce the effects of noise and IR drop between logic ground and battery ground, these drivers are designed to operate with a common-mode input range of ±20 V referenced to battery ground. The common-mode input voltages for the four drivers can be different, so a wide range of input elements can be accommodated. The high-impedance inputs are compatible with positive TTL and CMOS levels or negative logic levels. A clamp network is included in the driver outputs to limit high-voltage transients generated by the relay coil during switching. The complementary inputs ensure that the driver output is off as a fail-safe condition when either output is open.

The DS3680 is characterized for operation from 0°C to 70°C.

symbol (each driver)



schematic diagram (each driver)



All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range at BAT NEG, V_{BAT-} (see Note 1) . . . . . –70 V to 0.5 V
Input voltage range with respect to BAT GND . . . . . –70 V to 20 V
Input voltage range with respect to BAT NEG . . . . . –0.5 V to 70 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±20 V
Output current, I_O: Resistive load . . . . . –100 mA
Inductive load . . . . . –50 mA
Inductive output load . . . . . 5 H
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds . . . . . 260°C

NOTES: 1. All voltages are with respect to BAT GND, unless otherwise specified.
2. Differential input voltages are at the noninverting input terminal IN+ with respect to the inverting input terminal IN–.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{BAT-}	–10	–60	V
Input voltage, either input	–20†	20	V
High-level differential input voltage, V_{IDH}	2	20	V
Low-level differential input voltage, V_{IDL}	–20†	0.8	V
Operating free-air temperature, T_A	0	70	°C

† The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for input voltage levels.

electrical characteristics over recommended operating free-air temperature range, V_{BAT-} = –52 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
I_{IH}	High-level input current (into IN+)	V_{ID} = 2 V			40	100	µA
		V_{ID} = 7 V			375	1000	
I_{IL}	Low-level input current (into IN+)	V_{ID} = 0.4 V			0.01	5	µA
		V_{ID} = – 7 V			–1	–100	
$V_{O(on)}$	On-stage output voltage	I_O = 50 mA,	V_{ID} = 2 V		–1.6	–2.1	V
$I_{O(off)}$	Off-stage output current	$V_O = V_{BAT-}$	V_{ID} = 0.8 V		–2	–100	µA
			Inputs open		– 2	–100	
I_R	Clamp diode reverse current	V_O = 0			2	100	µA
V_{OK}	Output clamp voltage	I_O = 50 mA			0.9	1.2	V
		I_O = –50 mA,	V_{BAT-} = 0		–0.9	–1.2	
$I_{BAT(on)}$	On-state battery current	All drivers on			–2	–4.4	mA
$I_{BAT(off)}$	Off-state battery current	All drivers off			–1	–100	µA

‡ All typical values are at T_A = 25°C.

switching characteristics $V_{BAT–}$ = –52 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{on}	Turn-on time	V_{ID} = 3-V pulse, R_L = 1 kΩ, L = 1 H, See Figure 2		1	10	µs
t_{off}	Turn-off time			1	10	µs

PARAMETER MEASUREMENT INFORMATION

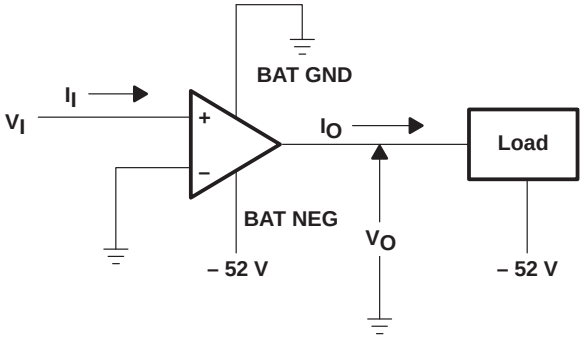


Figure 1. Generalized Test Circuit, Each Driver

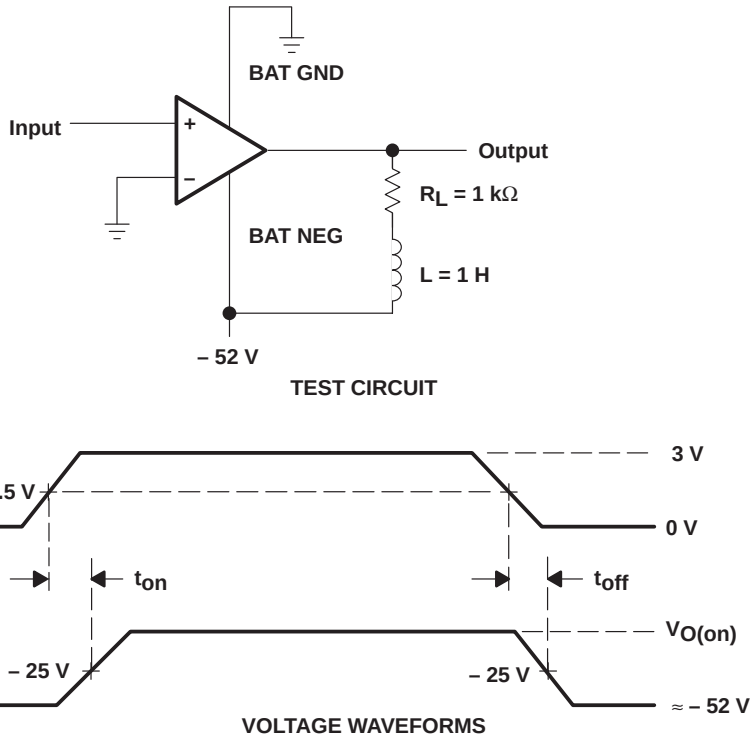


Figure 2. Test Circuit and Voltage Waveforms, Each Driver

APPLICATION INFORMATION

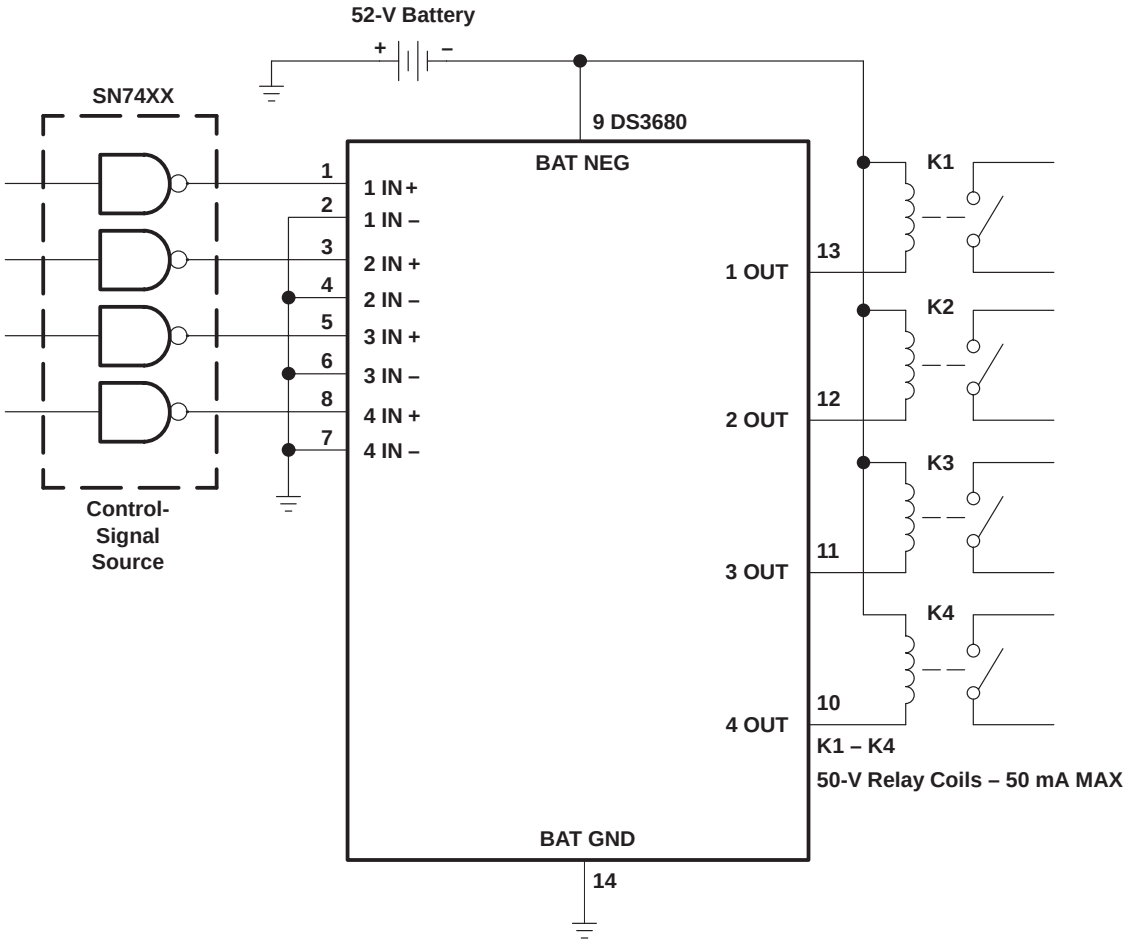


Figure 3. Relay Driver

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS3680D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	DS3680	Samples
DS3680DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	DS3680	Samples
DS3680N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	DS3680N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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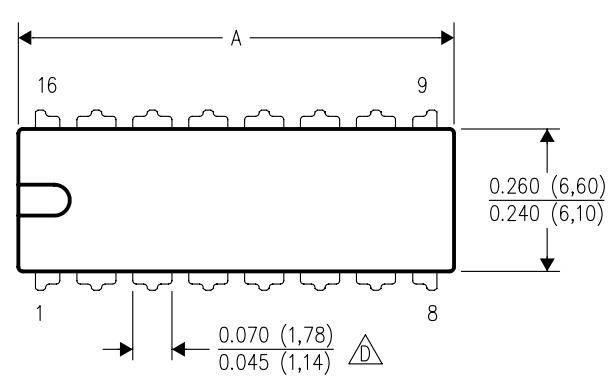
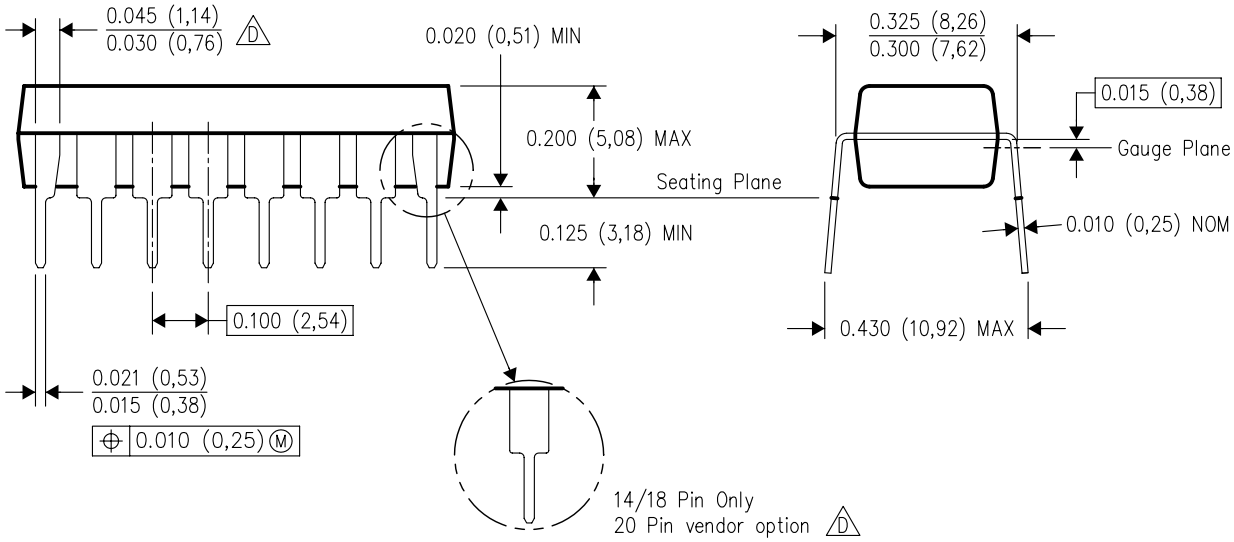
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



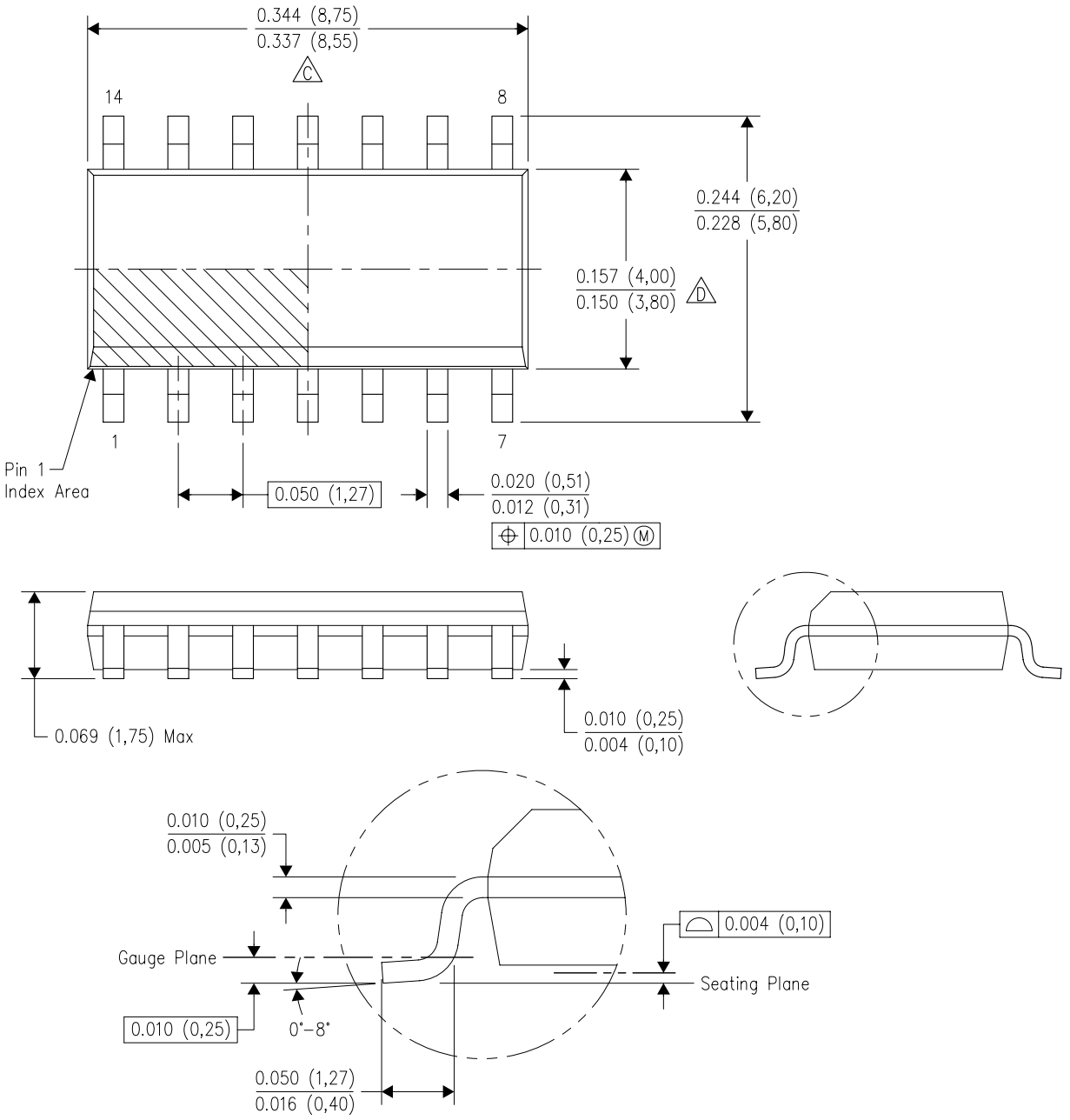
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

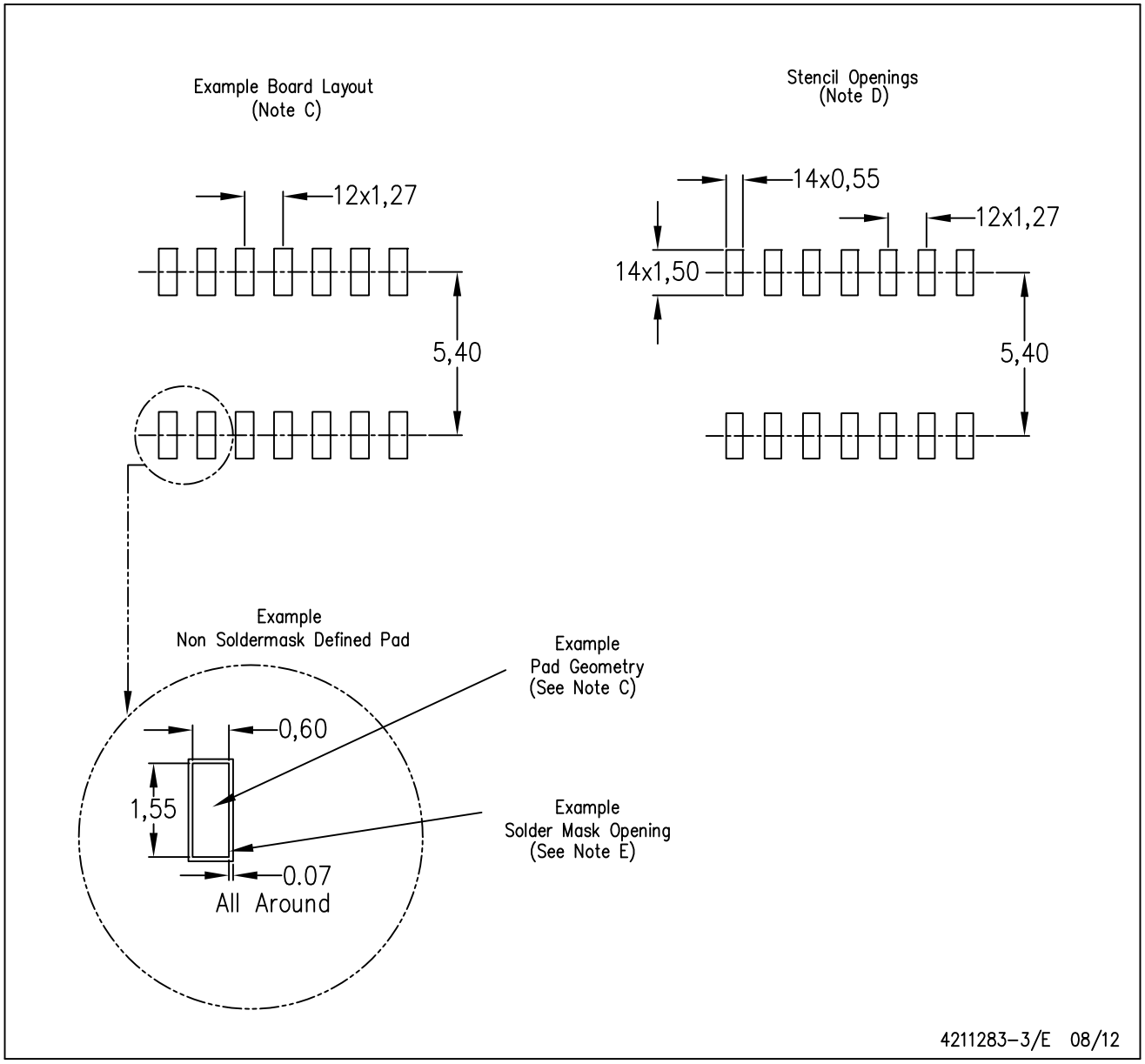
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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