MC68681

Advance Information

Dual Asynchronous Receiver/Transmitter

The MC68681 dual universal asynchronous receiver/transmitter (DUART) is part of the M68000 Family of peripherals and directly interfaces to the MC68000 processor via an asynchronous bus structure. The MC68681 consists of eight major sections: internal control logic, timing logic, interrupt control logic, a bidirectional 8-bit data bus buffer, two independent communication channels (A and B), a 6-bit parallel input port, and an 8-bit parallel output port (see Figure 1).

The following features are included on the MC68681:

- M68000 Bus Compatible
- Two, Independent, Full-Duplex Asynchronous Receiver/Transmitter Channels
- Maximum Data Transfer
  - 1X — 1 Mbps
  - 16X — 125 kbps
- Quadruple-Buffered Receiver Data Registers
- Double-Buffered Transmitter Data Registers
- Independently Programmable Baud Rate for Each Receiver and Transmitter Selectable from:
  - 18 Fixed Rates: 50 to 38.4k Baud
  - One User-Defined Rate Derived from a Programmable Timer/Counter
  - External 1X Clock or 16X Clock
- Programmable Data Format
  - Five to Eight Data Bits plus Parity
  - Odd, Even, No Parity, or Force Parity
  - One, One and One-Half, or Two Stop Bits Programmable in One-Sixteenth-Bit Increments
- Programmable Channel Modes
  - Normal (Full Duplex)
  - Automatic Echo
  - Local Loopback
  - Remote Loopback

- Automatic Wakeup Mode for Multidrop Applications
- Multifunction 6-Bit Input Port
  - Can Serve as Clock or Control Inputs
  - Change-of-State Detection on Four Inputs
- Multifunction 8-Bit Output Port
  - Individual Bit Set/Reset Capability
  - Outputs Can Be Programmed To Be Status/Interrupt Signals
- Multifunction 16-Bit Programmable Counter/Timer
- Versatile Interrupt System
  - Single Interrupt Output with Eight Maskable Interrupting Conditions
  - Interrupt Vector Output on Interrupt Acknowledge
  - Output Port Can Be Configured To Provide a Total of up to Six Separate Wire-ORable Interrupt Outputs

FEATURES (Continued)

- Parity, Framing, and Overrun Error Detection
- False-Start Bit Detection
- Line-Break Detection and Generation
- Detects Break Originating in the Middle of a Character
- Start/End Break Interrupt/Status
- On-Chip Crystal Oscillator
- TTL Compatible
- Single +5-V Power Supply

INTERNAL CONTROL LOGIC

The internal control logic receives operation commands from the central processing unit (CPU) and generates appropriate signals to the internal sections to control device operation. It allows the registers within the DUART to be accessed and various commands to be performed by decoding the four register select lines (RS1–RS4). In addition to the four register select lines, there are three inputs to the internal control logic from the CPU: read/write (R/$\overline{W}$), which allows read and write transfers between the CPU and DUART via the data bus buffer; chip select ($\overline{CS}$), which is the DUART chip select; and reset ($\overline{RESET}$), which is used to initialize or reset the DUART. The data transfer acknowledge ($\overline{DTACK}$) signal, asserted during read, write, or interrupt acknowledge is an output from the internal control logic. $\overline{DTACK}$ indicates to the CPU that data has been latched on a CPU write cycle or that valid data is present on the data bus during a CPU read cycle or interrupt acknowledge ($\overline{IACK}$) cycle.

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TIMING LOGIC

The timing logic consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer, and four clock selectors. The crystal oscillator operates directly from a 3.6864-MHz crystal connected across X1/CLK and X2 or from an external clock of the appropriate frequency connected to X1/CLK. The clock serves as the basic timing reference for the baud rate generator, the counter/timer, and other internal circuits. A clock signal within the limits given in **ELECTRICAL SPECIFICATIONS** must always be supplied to the DUART.

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communication baud rates ranging from 50 to 38.4k by producing internal clock outputs at 16 times

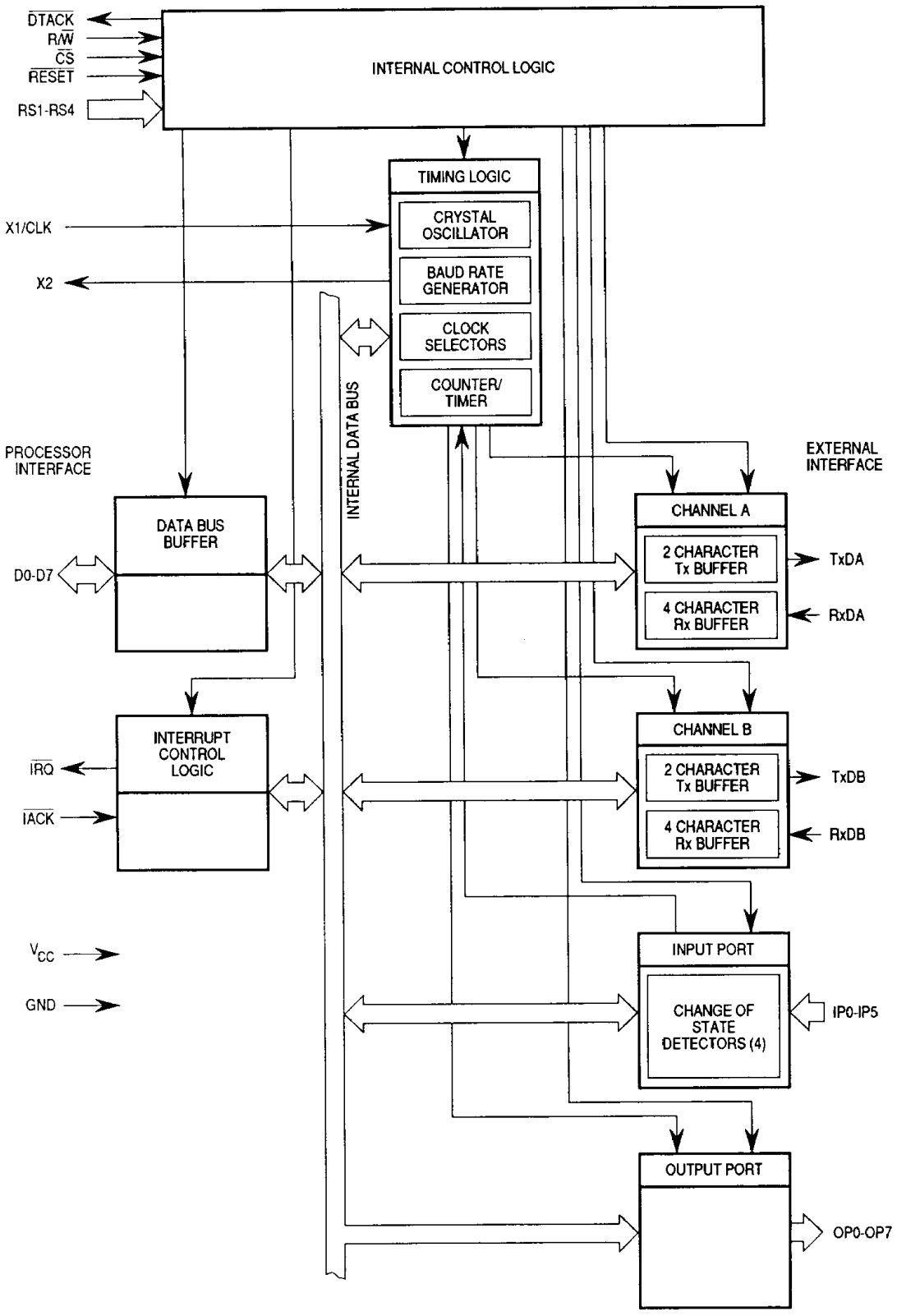

Figure 1. Block Diagram

the actual baud rate. The counter/timer can be used in the timer mode to produce a 16X clock for any other baud rate by counting down the crystal clock or external clock. Other baud rates may also be derived by connecting 16X or 1X clocks to certain input port pins that have alternate functions as receiver or transmitter clock inputs. The four clock selectors allow each receiver and transmitter to independently select any of these baud rates.

The 16-bit counter/timer included within the DUART and timing logic can be programmed to use one of several timing sources as input. The output of the counter/timer, which is available to the internal clock selectors, can also be programmed to be a parallel output at OP3. In the timer mode, the counter/timer acts as a programmable divider and can be used to generate a square-wave output at OP3. In the counter mode, the contents of the counter/timer can be read by the CPU, and it can be stopped and started under program control. The counter counts down the number of pulses stored in the concatenation of the counter/timer upper register and counter/timer lower register and produces an interrupt. This system-oriented feature may be used to keep track of timeouts when implementing various application protocols.

INTERRUPT CONTROL LOGIC

The following registers are associated with the interrupt control logic: interrupt mask register (IMR), interrupt status register (ISR), auxiliary control register (ACR), and interrupt vector register (IVR).

An active-low interrupt request ($\overline{IRQ}$) can be used to notify the processor that any of eight internal events has occurred. The IMR can be programmed to select only certain conditions that cause $\overline{IRQ}$ to be asserted; the ISR can be read by the CPU to determine all currently active interrupting conditions. When an active-low $\overline{IACK}$ from the processor is assserted while the DUART has an interrupt pending, the DUART will place the contents of the IVR (i.e., the interrupt vector) on the data bus and assert $\overline{DTACK}$.

In addition, the DUART offers the ability to program the parallel outputs OP3–OP7 to provide discrete interrupt outputs for the transmitters, the receivers, and the counter/timer.

DATA BUS BUFFER

The data bus buffer, which provides the interface between the external and internal data buses, is controlled by the internal control logic to allow read and write data transfer operations to occur between the controlling CPU and DUART via the eight parallel data lines (D0–D7).

COMMUNICATION CHANNELS A AND B

Each communication channel comprises a full-duplex universal asynchronous receiver/transmitter (UART). The operating frequency for each receiver and each transmitter can be independently selected from the baud rate generator, the counter/timer, or an external clock.

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits, and outputs a composite serial stream of data on the TxD output pin. The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for a start bit, stop bit, parity bit (if any), or break condition, and transfers an assembled character to the CPU during read operations.

INPUT PORT

The inputs to this unlatched 6-bit port (IP0–IP5) can be read by the CPU during a read operation. High or low inputs to the input port result in the CPU reading a logic one or logic zero, respectively; that is, there is no inversion of the logic level. Since the input port is a 6-bit port, performing a read operation will result in D7 being read as a logic one and D6 reflecting the logic level of $\overline{\text{IACK}}$. Besides functioning as general-purpose inputs, the inputs to this port can be individually assigned specific auxiliary functions serving the communication channels.

Four change-of-state detectors, also provided within the input port, are associated with inputs IP0, IP1, IP2, and IP3. A high-to-low or low-to-high transition of these inputs lasting longer than 25 to 30 μs (best-to-worst times) will set the corresponding bit in the input port change register (IPCR). The bits are cleared when the register is read by the CPU. Also, the DUART can be programmed so any particular change of state can generate an interrupt to the CPU. The DUART internally recognizes a level change on an input pin after it has sampled the new level on the pin for two successive pulses of the sampling clock. The sampling clock is 38.4 kHz and is derived from one of the baud rate generator taps. The resulting sampling period is slightly more than 25 μs (assuming a

clock input of 3.6864 MHz). Subsequently, if the level change occurs on or just before a sampling pulse, it will be recognized internally after 25 μs. However, if the level change occurs just after a sampling pulse, it will be sampled the first time after 25 μs. Thus, in this case, the level change will not be recognized internally until 50 μs after the level change occurred on the pin.

OUTPUT PORT

This 8-bit multipurpose output port can be used as a general-purpose output port. All bits of the output port register (OPR) can be individually set and reset. A bit is set by performing a write operation at the appropriate address with the accompanying data specifying the bits to be set (one equals set and zero equals no change). Similarly, a bit is reset by performing a write operation at another address with the accompanying data specifying the bits to be reset (one equals reset and zero equals no change).

The OPR stores data that is to be output at the output port pins. Unlike the input port, if a particular bit of the OPR is set to a logic one or logic zero, the output pin will be at a low or high level, respectively. Thus, a *logic inversion* occurs internal to the DUART with respect to this register. The outputs are complements of the data contained in the OPR.

Besides functioning as general-purpose outputs, the outputs can be individually assigned specific auxiliary functions serving the communication channels. The assignment is accomplished by appropriately programming the channel A and B mode registers (MR1A, MR1B, MR2A, and MR2B) and the output port configuration register (OPCR).

SIGNAL DESCRIPTION

The following paragraphs contain a brief description of the input and output signals.

NOTE

The terms **assertion** and **negation** will be used extensively to avoid confusion when dealing with a mixture of active-low and active-high signals. The term assert or assertion is used to indicate that a signal is active or true, independent of whether that level is represented by a high or low voltage. The term negate or negation is used to indicate that a signal is inactive or false.

V_{CC} AND GND

Power is supplied to the DUART using these two signals. V_{CC} is power (+5 V) and GND is the ground connection.

CRYSTAL INPUT OR EXTERNAL CLOCK (X1/CLK)

This input is one of two connections to a crystal or a connection to an external clock. A crystal or a clock within the specified limits must be supplied at all times. If a crystal is used, a capacitor of approximately 10 to 15 pF should be connected from this pin to GND.

CRYSTAL OUTPUT (X2)

This output is an additional connection to a crystal. If an external TTL-level clock is used, this pin should be tied to GND. If a crystal is used, a capacitor of approximately 0 to 5 pF should be connected from this pin to GND.

RESET ($\overline{\text{RESET}}$)

The DUART can be reset by asserting the $\overline{\text{RESET}}$ signal or by programming the appropriate command register. A hardware reset, assertion of $\overline{\text{RESET}}$, clears status registers A and B (SRA and SRB), the IMR, the ISR, the OPR, and the OPCR. $\overline{\text{RESET}}$ initializes the IVR to $0F, places parallel outputs OP0–OP3 in the high state, places the counter/timer in timer mode, and places channels A and B in the inactive state with the channel A transmitter serial data output (TxDA) and channel B transmitter serial data output (TxDB) in the mark (high) state.

Software resets are not as encompassing and are achieved by appropriately programming the channel A and/or B command register. Reset commands can be programmed through the command register to reset the receiver, transmitter, error status, or break-change interrupts for each channel.

CHIP SELECT ($\overline{\text{CS}}$)

This active-low input signal, when low, enables data transfers between the CPU and DUART on D0–D7. These data transfers are controlled by R/$\overline{\text{W}}$ and the register select inputs (RS1–RS4). When $\overline{\text{CS}}$ is high, D0–D7 are placed in the high-impedance state.

READ/WRITE (R/$\overline{W}$)

When high, this input indicates a read cycle, and when low, it indicates a write cycle. A cycle is initiated by assertion of $\overline{CS}$.

DATA TRANSFER ACKNOWLEDGE ($\overline{DTACK}$)

This three-state, active-low, open-drain output is asserted in read, write, or interrupt acknowledge cycles to indicate the proper transfer of data between the CPU and DUART.

REGISTER SELECT BUS (RS1–RS4)

The register select bus lines during read/write operations select the DUART internal registers, ports, or commands.

DATA BUS (D0–D7)

These bidirectional three-state data lines are used to transfer commands, data, and status between the CPU and DUART. D0 is the least significant bit.

INTERRUPT REQUEST ($\overline{IRQ}$)

This active-low open-drain output signals the CPU that one or more of the eight maskable interrupting conditions are true.

INTERRUPT ACKNOWLEDGE ($\overline{IACK}$)

This active-low input indicates an interrupt acknowledge cycle. If an interrupt is pending ($\overline{IRQ}$ asserted) and this pin is asserted, the DUART responds by placing the interrupt vector on the data bus and then asserting $\overline{DTACK}$. If there is no interrupt pending ($\overline{IRQ}$ negated), the DUART ignores the status of this pin.

CHANNEL A TRANSMITTER SERIAL DATA OUTPUT (TxDA)

This signal is the transmitter serial data output for channel A. This output is held high (mark condition) when the transmitter is disabled, idle, or operating in the local loopback mode. (Mark is high and space is low.) Data is shifted out of TxDA on the falling edge of the programmed clock source, with the least significant bit transmitted first.

CHANNEL A RECEIVER SERIAL DATA INPUT (RxDA)

This signal is the receiver serial data input for channel A. Data on RxDA is sampled on the rising edge of the programmed clock source, with the least significant bit received first.

CHANNEL B TRANSMITTER SERIAL DATA OUTPUT (TxDB)

This signal is the transmitter serial data output for channel B. The output is held high (mark condition) when the transmitter is disabled, idle, or operating in the local loopback mode. Data is shifted out of TxDB on the falling edge of the programmed clock source, with the least significant bit transmitted first.

CHANNEL B RECEIVER SERIAL DATA INPUT (RxDB)

This signal is the receiver serial data input for channel B. Data on RxDB is sampled on the rising edge of the programmed clock source, with the least significant bit received first.

PARALLEL INPUTS (IP0–IP5)

Each parallel signal can be used as a general-purpose input. However, each input has an alternate function(s), which is described in the following paragraphs.

IP0 This signal can be used as the channel A clear-to-send active-low input ($\overline{\text{CTSA}}$). A change-of-state detector is also associated with this input.

IP1 This signal can be used as the channel B clear-to-send active-low input ($\overline{\text{CTSB}}$). A change-of-state detector is also associated with this input.

IP2 This signal can be used as the channel B receiver external clock input (RxCB) or as the counter/timer external clock input. When this input is used as the external clock by the receiver, the received data is sampled on the rising edge of the clock. A change-of-state detector is also associated with this input.

IP3 This signal can be used as the channel A transmitter external clock input (TxCA). When this input is used as the external clock by the transmitter, the transmitted data is clocked on the falling edge of the clock. A change-of-state detector is also associated with this input.

IP4 This signal can be used as the channel A receiver external clock input (RxCA). When this input is used as the external clock by the receiver, the received data is sampled on the rising edge of the clock.

IP5 This signal can be used as the channel B transmitter external clock input (TxCB). When this input is used as the external clock by the transmitter, the transmitted data is clocked on the falling edge of the clock.

PARALLEL OUTPUTS (OP0–OP7)

Each parallel signal can be used as a general-purpose output. However, each output has an alternate function(s), which is described in the following paragraphs.

OP0 This signal can be used as the channel A active-low request-to-send output ($\overline{\text{RTSA}}$). When used for this function, it is automatically negated and reasserted by either the receiver or transmitter.

OP1 This signal can be used as the channel B active-low request-to-send output ($\overline{\text{RTSB}}$). When used for this function, it is negated and reasserted automatically by either the receiver or transmitter.

OP2 This signal can be used as the channel A transmitter 1X clock or 16X clock output or as the channel A receiver 1X clock output.

OP3 This signal can be used as the open-drain active-low counter-ready output, the open-drain timer output, the channel B transmitter 1X clock output, or the channel B receiver 1X clock output.

OP4 This signal can be used as the channel A open-drain active-low receiver-ready or buffer-full interrupt outputs ($\overline{\text{RxRDYA}}$/$\overline{\text{FFULLA}}$) by appropriately programming bit 6 of MR1A.

OP5 This signal can be used as the channel B open-drain active-low receiver-ready or buffer-full interrupt outputs ($\overline{\text{RxRDYB}}$/$\overline{\text{FFULLB}}$) by appropriately programming bit 6 of MR1B.

OP6 This signal can be used as the channel A open-drain active-low transmitter-ready interrupt output ($\overline{\text{TxRDYA}}$) by appropriately programming bit 6 of the OPCR.

OP7 This signal can be used as the channel B open-drain active-low transmitter-ready interrupt output ($\overline{\text{TxRDYB}}$) by appropriately programming bit 7 of the OPCR.

SIGNAL SUMMARY

Table 1 provides a summary of all MC68681 signals.

Table 1. Signal Summary

Signal Name	Mnemonic	Pin No.	Input/Output	Active State
Power Supply (+5 V)	V_{CC}	40	Input	High
Ground	GND	20	Input	Low
Crystal Input or External Clock	X1/CLK	32	Input	—
Crystal Output	X2	33	Output	—
Reset	$\overline{\text{RESET}}$	34	Input	Low
Chip Select	$\overline{\text{CS}}$	35	Input	Low
Read/Write	R/$\overline{\text{W}}$	8	Input	High/Low
Data Transfer Acknowledge	$\overline{\text{DTACK}}$	9	Output*	Low
Register Select Bus Bit 4	RS4	6	Input	—
Register Select Bus Bit 3	RS3	5	Input	—
Register Select Bus Bit 2	RS2	3	Input	—
Register Select Bus Bit 1	RS1	1	Input	—
Bidirectional Data Bus Bit 7	D7	19	Input/Output	—
Bidirectional Data Bus Bit 6	D6	22	Input/Output	—
Bidirectional Data Bus Bit 5	D5	18	Input/Output	—
Bidirectional Data Bus Bit 4	D4	23	Input/Output	—
Bidirectional Data Bus Bit 3	D3	17	Input/Output	—
Bidirectional Data Bus Bit 2	D2	24	Input/Output	—
Bidirectional Data Bus Bit 1	D1	16	Input/Output	—
Bidirectional Data Bus Bit 0 (Least Significant Bit)	D0	25	Input/Output	—
Interrupt Request	$\overline{\text{IRQ}}$	21	Output*	Low
Interrupt Acknowledge	$\overline{\text{IACK}}$	37	Input	Low
Channel A Transmitter Serial Data	TxDA	30	Output	—
Channel A Receiver Serial Data	RxDA	31	Input	—
Channel B Transmitter Serial Data	TxDB	11	Output	—
Channel B Receiver Serial Data	RxDB	10	Input	—
Parallel Input 5	IP5	38	Input	—
Parallel Input 4	IP4	39	Input	—
Parallel Input 3	IP3	2	Input	—
Parallel Input 2	IP2	36	Input	—
Parallel Input 1	IP1	4	Input	—
Parallel Input 0	IP0	7	Input	—

Table 1. Signal Summary (Continued)

Signal Name	Mnemonic	Pin No.	Input/Output	Active State
Parallel Output 7	OP7	15	Output**	—
Parallel Output 6	OP6	26	Output**	—
Parallel Output 5	OP5	14	Output**	—
Parallel Output 4	OP4	27	Output**	—
Parallel Output 3	OP3	13	Output**	—
Parallel Output 2	OP2	28	Output	—
Parallel Output 1	OP1	12	Output	—
Parallel Output 0	OP0	29	Output	—

*Requires a pullup resistor.
**May require a pullup resistor, depending upon its programmed function.

PROGRAMMING AND REGISTER DESCRIPTION

The operation of the DUART is programmed by writing control words into the appropriate registers. Operational feedback is provided by the status registers, which can be read by the CPU. The DUART register address and address-triggered commands are described in Table 2.

Table 2. Register Addressing and Address-Triggered Commands

RS4	RS3	RS2	RS1	Read (R/$\overline{W}$ = 1)	Write (R/$\overline{W}$ = 0)
0	0	0	0	Mode Register A (MR1A, MR2A)	Mode Register A (MR1A, MR2A)
0	0	0	1	Status Register A (SRA)	Clock Select Register A (CSRA)
0	0	1	0	Do Not Access*	Command Register A (CRA)
0	0	1	1	Receiver Buffer A (RBA)	Transmitter Buffer A (TBA)
0	1	0	0	Input Port Change Register (IPCR)	Auxiliary Control Register (ACR)
0	1	0	1	Interrupt Status Register (ISR)	Interrupt Mask Register (IMR)
0	1	1	0	Counter Mode: Current MSB of Counter (CUR)	Counter/Timer Upper Register (CTUR)
0	1	1	1	Counter Mode: Current LSB of Counter (CLR)	Counter/Timer Lower Register (CTLR)
1	0	0	0	Mode Register B (MR1B, MR2B)	Mode Register B (MR1B, MR2B)
1	0	0	1	Status Register B (SRB)	Clock Select Register B (CSRB)
1	0	1	0	Do Not Access*	Command Register B (CRB)
1	0	1	1	Receiver Buffer B (RBB)	Transmitter Buffer B (TBB)
1	1	0	0	Interrupt Vector Register (IVR)	Interrupt Vector Register (IVR)
1	1	0	1	Input Port (Unlatched)	Output Port Configuration Register (OPCR)
1	1	1	0	Start Counter Command**	Output Port Register (OPR) Bit Set Command**
1	1	1	1	Stop Counter Command**	Output Port Register (OPR) Bit Reset Command**

*This address location is used for factory testing of the DUART and should not be read. Reading this location will result in undesired effects and possible incorrect transmission or reception of characters. Register contents may also be changed.
**Address-triggered commands.

Figure 2 illustrates a block diagram of the DUART from a programming standpoint and details the register configuration for each block. The locations marked "do not access" should never be read during normal operation. They are used by the factory for testing purposes.

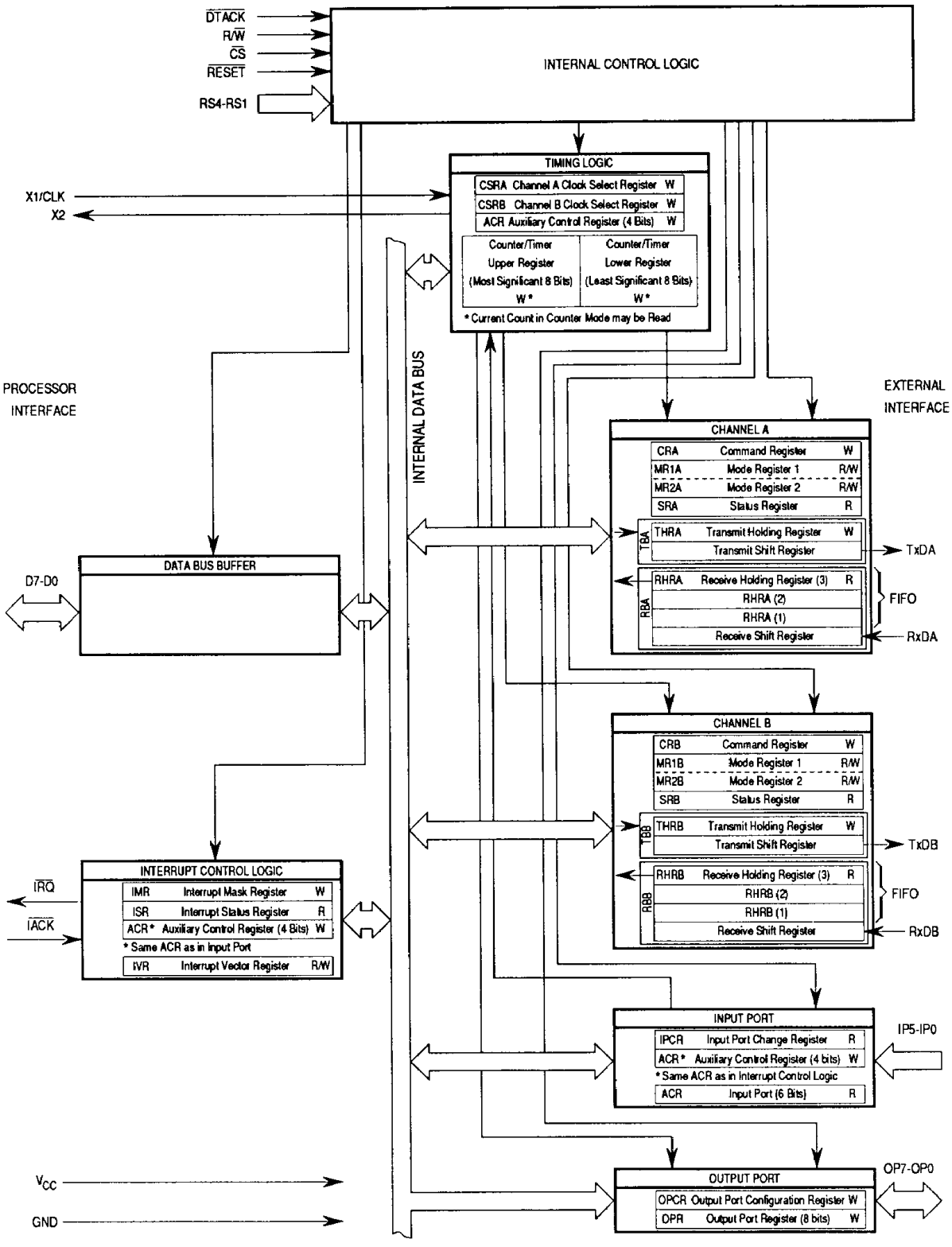

Figure 2. Programming Block Diagram

Tables 3 and 4 list the various input port pin functions and output port pin functions, respectively.

Table 3. Programming of Input Port Functions

Function	Input Port Pin					
	IP5	IP4	IP3	IP2	IP1	IP0
General Purpose	Default	Default	Default	Default	Default	Default
Change-of-State Detector			Default	Default	Default	Default
External Counter 1X Clock Input				ACR[6:4] = 000		
External Timer 16X Clock Input				ACR[6:4] = 100		
External Timer 1X Clock Input				ACR[6:4] = 101		
RxCA 16X		CSRA[7:4] = 1110				
RxCA 1X		CSRA[7:4] = 1111				
TxCA 16X			CSRA[3:0] = 1110			
TxCA 1X			CSRA[3:0] = 1111			
RxCB 16X				CSRB[7:4] = 1110		
RxCB 1X				CSRB[7:4] = 1111		
TxCB 16X	CSRB[3:0] = 1110					
TxCB 1X	CSRB[3:0] = 1111					
TxCTSA						MR2A[4] = 1
TxCTSB					MR2B[4] = 1	

*In these modes, because IP2 is used for the counter/timer clock input, it is not available for use as the channel B receiver clock input.

NOTE: Default refers to the function the input port pins perform when not used in one of the other modes. Only those functions which show the register programming are available for use.

Table 4. Programming of Output Port Functions

Function	Output Port Pin							
	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
General Purpose	OPCR[7] = 0	OPCR[6] = 0	OPCR[5] = 0	OPCR[4] = 0	OPCR[3:2] = 00	OPCR[1:0] = 00	MR1B[7] = 0 MR2B[5] = 0	MR1A[7] = 0 MR2A[5] = 0
$\overline{\text{CTRDY}}$					OPCR[3:2] = 01, ACR[6] = 0*			
Timer Output					OPCR[3:2] = 01, ACR[6] = 1*			
TxCB 1X					OPCR[3:2] = 10			
RxCB 1X					OPCR[3:2] = 11			
TxCA 16X						OPCR[1:0] = 01		
TxCA 1X						OPCR[1:0] = 10		
RxCA 1X						OPCR[1:0] = 11		
$\overline{\text{TxRDYA}}$		OPCR[6] = 1*						
$\overline{\text{TxRDYB}}$	OPCR[7] = 1*							
$\overline{\text{RxRDYA}}$				OPCR[4] = 1, MR1A[6] = 0*				
$\overline{\text{RxRDYB}}$			OPCR[5] = 1, MR1B[6] = 0*					
$\overline{\text{FFULLA}}$				OPCR[4] = 1, MR1A[6] = 1				
$\overline{\text{FFULLB}}$			OPCR[5] = 1, MR1B[6] = 1*					
$\overline{\text{RxRTSA}}$								MR1A[7] = 1
$\overline{\text{TxRTSA}}$								MR2A[5] = 1
$\overline{\text{RxRTSB}}$							MR1B[7] = 1	
$\overline{\text{TxRTSB}}$							MR2B[5] = 1	

NOTE: Only those functions showing the register programming are available for use.
*Pin requires a pullup resistor if used for this function.

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Table 5 lists the various clock sources that may be selected for the counter and timer. More detailed information is provided in Table 6.

Table 5. Selection of Clock Sources for the Counter and Timer Modes

Counter Mode Clock Sources (ACR[6]=0)	ACR[5:4]=
External Input via Input Port Pin 2 (IP2)	00
Channel A 1X Transmitter Clock TxCA	01
Channel B 1X Transmitter Clock TxCB	10
Crystal Oscillator Divide by 16 via X1/Clk and X2	11
External Input Divide by 16 via X1/CLK Input Pin	11

NOTE: Only those functions showing the register programming are available for use.

Timer Mode Clock Sources (ACR[6]=1)	ACR[5:4]=
External Input via Input Port Pin 2 (IP2)	00
External Input Divide by 16 via Input Port Pin 2 (IP2)	01
Crystal Oscillator via X1/CLK and X2	10
Crystal Oscillator Divide by 16 via X1/CLK and X2	11
External Input via X1/CLK Input Pin	10
External Input Divide by 16 via X1/CLK Input Pin	11

Care should be exercised if register contents are changed during receiver/transmitter operation since certain changes may cause undesired results. For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. The contents of the mode registers, the clock select register (CSR), the OPCR, and bit 7 of the ACR should only be changed after the receiver(s) and transmitter(s) have been issued software Rx and Tx reset commands. Similarly, certain changes to ACR bits 6–4 should only be made while the counter/timer is not used (i.e., stopped if in counter mode; output and/or interrupt masked in timer mode).

Mode registers 1 and 2 of each channel are accessed via independent auxiliary pointers. The pointer is set to channel A mode register 1 (MR1A) and channel B mode register 1 (MR1B) by $\overline{\text{RESET}}$ or by issuing a "reset pointer" command via the corresponding command register. Any read or write of the mode register while the pointer is at MR1A or MR1B switches the pointer to channel A mode register 2 (MR2A) or channel B mode register 2 (MR2B). The pointer then remains at MR2A or MR2B. Subsequent accesses will address MR2A or MR2B unless the pointer is reset to MR1A or MR1B.

Mode, command, clock select, and status registers are duplicated for each channel to provide independent operation and control. Refer to Table 6 for descriptions of the registers.

Table 6. Register Bit Formats

CHANNEL A MODE REGISTER 1 (MR1A) AND CHANNEL B MODE REGISTER 1 (MR1B)

Rx RTS Control	Rx $\overline{IRQ}$ Select	Error Mode	Parity Mode	Parity Type	Bits-per-Character
Bit 7	Bit 6	Bit 5	Bit 4 Bit 3	Bit 2	Bit 1 Bit 0
				With Parity 0 = Even 1 = Odd	
0 = Disabled 1 = Enabled	0 = RxRDY 1 = FFULL	0 = Char 1 = Block	0 0 = With Parity 0 1 = Force Parity 1 0 = No Parity 1 1 = Multidrop Mode*	Force Parity 0 = Low 1 = High	0 0 = 5 0 1 = 6 1 0 = 7 1 1 = 8
				Multidrop Mode 0 = Data 1 = Address	

*The parity bit is used as the address/data bit in multidrop mode.

CHANNEL A MODE REGISTER 2 (MR2A) AND CHANNEL B MODE REGISTER 2 (MR2B)

Channel Mode	Tx RTS Control	CTS Enable Transmitter	Stop Bit Length		
Bit 7 Bit 6	Bit 5	Bit 4	Bit 3 Bit 2 Bit 1 Bit 0	6-8 Bits/ Character	5-Bits/ Character
0 0 = Normal	0 = Disabled	0 = Disabled	(0) 0 0 0 0 =	0.563	1.063
0 1 = Automatic Echo	1 = Enabled	1 = Enabled	(1) 0 0 0 1 =	0.625	1.125
1 0 = Local Loopback			(2) 0 0 1 0 =	0.688	1.188
1 1 = Remote Loopback			(3) 0 0 1 1 =	0.750	1.250
			(4) 0 1 0 0 =	0.813	1.313
			(5) 0 1 0 1 =	0.875	1.375
			(6) 0 1 1 0 =	0.938	1.438
			(7) 0 1 1 1 =	1.000	1.500
			(8) 1 0 0 0 =	1.563	1.563
			(9) 1 0 0 1 =	1.625	1.625
			(A) 1 0 1 0 =	1.688	1.688
			(B) 1 0 1 1 =	1.750	1.750
			(C) 1 1 0 0 =	1.813	1.813
			(D) 1 1 0 1 =	1.875	1.875
			(E) 1 1 1 0 =	1.938	1.938
			(F) 1 1 1 1 =	2.000	2.000

NOTE:
If an external 1X clock is used for the transmitter, MR2 bit 3 = 0 selects one stop bit and MR2 bit 3 = 1 selects two stop bits to be transmitted.

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Table 6. Register Bit Formats (Continued)

CLOCK-SELECT REGISTER A (CSRA)

Receiver-Clock Select			Transmitter-Clock Select		
Bit 7 Bit 6 Bit 5 Bit 4	Baud Rate		Bit 3 Bit 2 Bit 1 Bit 0	Baud Rate	
	Set 1 ACR Bit 7=0	Set 2 ACR Bit 7=1		Set 1 ACR Bit 7=0	Set 2 ACR Bit 7=1
0 0 0 0	50	75	0 0 0 0	50	75
0 0 0 1	110	110	0 0 0 1	110	110
0 0 1 0	134.5	134.5	0 0 1 0	134.5	134.5
0 0 1 1	200	150	0 0 1 1	200	150
0 1 0 0	300	300	0 1 0 0	300	300
0 1 0 1	600	600	0 1 0 1	600	600
0 1 1 0	1200	1200	0 1 1 0	1200	1200
0 1 1 1	1050	2000	0 1 1 1	1050	2000
1 0 0 0	2400	2400	1 0 0 0	2400	2400
1 0 0 1	4800	4800	1 0 0 1	4800	4800
1 0 1 0	7200	1800	1 0 1 0	7200	1800
1 0 1 1	9600	9600	1 0 1 1	9600	9600
1 1 0 0	38.4k	19.2k	1 1 0 0	38.4k	19.2k
1 1 0 1	Timer	Timer	1 1 0 1	Timer	Timer
1 1 1 0	IP4-16X	IP4-16X	1 1 1 0	IP3-16X	IP3-16X
1 1 1 1	IP4-1X	IP4-1X	1 1 1 1	IP3-1X	IP3-1X

NOTE: Receiver clock is always a 16X clock except when CSRA bits 7–4 equal 1111.

NOTE: Transmitter clock is always a 16X clock except when CSRA bits 3–0 equal 1111.

CLOCK-SELECT REGISTER B (CSRB)

Receiver-Clock Select			Transmitter-Clock Select		
Bit 7 Bit 6 Bit 5 Bit 4	Baud Rate		Bit 3 Bit 2 Bit 1 Bit 0	Baud Rate	
	Set 1 ACR Bit 7=0	Set 2 ACR Bit 7=1		Set 1 ACR Bit 7=0	Set 2 ACR Bit 7=1
0 0 0 0	50	75	0 0 0 0	50	75
0 0 0 1	110	110	0 0 0 1	110	110
0 0 1 0	134.5	134.5	0 0 1 0	134.5	134.5
0 0 1 1	200	150	0 0 1 1	200	150
0 1 0 0	300	300	0 1 0 0	300	300
0 1 0 1	600	600	0 1 0 1	600	600
0 1 1 0	1200	1200	0 1 1 0	1200	1200
0 1 1 1	1050	2000	0 1 1 1	1050	2000
1 0 0 0	2400	2400	1 0 0 0	2400	2400
1 0 0 1	4800	4800	1 0 0 1	4800	4800
1 0 1 0	7200	1800	1 0 1 0	7200	1800
1 0 1 1	9600	9600	1 0 1 1	9600	9600
1 1 0 0	38.4k	19.2k	1 1 0 0	38.4k	19.2k
1 1 0 1	Timer	Timer	1 1 0 1	Timer	Timer
1 1 1 0	IP2-16X	IP2-16X	1 1 1 0	IP5-16X	IP5-16X
1 1 1 1	IP2-1X	IP2-1X	1 1 1 1	IP5-1X	IP5-1X

NOTE: Receiver clock is always a 16X clock except when CSRB bits 7–4 equal 1111.

NOTE: Transmitter clock is always a 16X clock except when CSRB bits 3–0 equal 1111.

Table 6. Register Bit Formats (Continued)

CHANNEL A COMMAND REGISTER (CRA) AND CHANNEL B COMMAND REGISTER (CRB)

Not Used*	Miscellaneous Commands	Transmitter Commands	Receiver Commands
Bit 7	Bit 6 Bit 5 Bit 4	Bit 3 Bit 2	Bit 1 Bit 0
X	0 0 0 No Command 0 0 1 Reset MR Pointer to MR1 0 1 0 Reset Receiver 0 1 1 Reset Transmitter 1 0 0 Reset Error Status 1 0 1 Reset Channel's Break Change Interrupt 1 1 0 Start Break 1 1 1 Stop Break	0 0 No Action, Stays in Present Mode 0 1 Transmitter Enabled 1 0 Transmitter Disabled 1 1 Don't Use, Indeterminate	0 0 No Action, Stays in Present Mode 0 1 Receiver Enabled 1 0 Receiver Disabled 1 1 Don't Use, Indeterminate

*Bit 7 is not used and may be set to either zero or one.

CHANNEL A STATUS REGISTER (SRA) AND CHANNEL B STATUS REGISTER (SRB)

Received Break	Framing Error	Parity Error	Overrun Error	TxEMT	TxRDY	FFULL	RxRDY
Bit 7*	Bit 6*	Bit 5*	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

*These status bits are appended to the corresponding data character in the receive FIFO and are valid only when RxRDY is set. A read of the status register provides these bits (7–5) from the top of the FIFO together with bits 4–0. These bits are cleared by a reset error status command. In character mode, they are discarded when the corresponding data character is read from the FIFO.

OUTPUT PORT CONFIGURATION REGISTER (OPCR)

OP7	OP6	OP5	OP4	OP3	OP2
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3 Bit 2	Bit 1 Bit 0
0 = OPR Bit 7 1 = TxRDYB	0 = OPR Bit 6 1 = TxRDYA	0 = OPR Bit 5 1 = RxRDYB / FFULLB	0 = OPR Bit 4 1 = RxRDYA/ FFULLA	0 0 = OPR Bit 3 0 1 = C/T Output * 1 0 = TxCB (1X) 1 1 = RxCB (1X)	0 0 = OPR Bit 2 0 1 = TxCA (16X) 1 0 = TXCA (1X) 1 1 = RxCA (1X)

*If OP3 is to be used for the timer output, the counter/timer should be programmed for timer mode (ACR[6] = 1), the counter/timer preload registers (CTUR and CTLR) initialized, and the start counter command issued before setting OPCR[3:2] = 01.

NOTE: OP1 and OP0 can be used as transmitter and receiver RTS control lines by appropriately programming the mode registers (MR1[7] for RxRTS and MR2[5] forTxRTS). OP1 is used for the channel B RTS control line and OP0 for the channel A RTS control line. When OP1 and OP0 are not used for RTS control, they may be used as general-purpose outputs.

OUTPUT PORT REGISTER (OPR)

OPR7	OPR6	OPR5	OPR4	OPR3	OPR2	OPR1	OPR0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Table 6. Register Bit Formats (Continued)

AUXILIARY CONTROL REGISTER (ACR)

BRG SET Select*	Counter/Timer Mode and Source**			Delta*** IP3 IRQ	Delta*** IP2 IRQ	Delta*** IP1 IRQ	Delta*** IP0 IRQ
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Mode		Clock Source				
0 = Set 1				0 = Disabled	0 = Disabled	0 = Disabled	0 = Disabled
1 = Set 2	0	0	0 Counter — External (IP2)****	1 = Enabled	1 = Enabled	1 = Enabled	1 = Enabled
	0	0	1 Counter — TxCA – 1X Clock of Channel A Transmitter				
	0	1	0 Counter — TxCB – 1X Clock of Channel B Transmitter				
	0	1	1 Counter — Crystal or External Clock (X1/CLK) Divided by 16				
	1	0	0 Timer — External (IP2)****				
	1	0	1 Timer — External (IP2) Divided by 16****				
	1	1	0 Timer — Crystal or External Clock (X1/CLK)				
	1	1	1 Timer — Crystal or External Clock (X1/CLK) Divided by 16				

* Should only be changed after both channels have been reset and are disabled.

** Should only be altered while the counter/timer is not in use (i.e., stopped if in counter mode, output and/or interrupt masked if in timer mode).

*** Delta is equivalent to change-of-state.

**** In these modes, because IP2 is used for the counter/timer clock input, it is not available for use as the channel B receiver-clock input.

INPUT PORT CHANGE REGISTER (IPCR)

Delta* Detected IP3	Delta* Detected IP2	Delta* Detected IP1	Delta* Detected IP0	Level IP3	Level IP2	Level IP1	Level IP0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 = No	0 = No	0 = No	0 = No	0 = Low	0 = Low	0 = Low	0 = Low
1 = Yes	1 = Yes	1 = Yes	1 = Yes	1 = High	1 = High	1 = High	1 = High

* Delta is equivalent to change-of-state.

INTERRUPT STATUS REGISTER (ISR)

Input Port Change	Delta Break B	RxRDYB/ FFULLB	TxRDYB	Counter/ Timer Ready	Delta Break A	RxRDYA/ FFULLA	TxRDYA
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 = No	0 = No	0 = No	0 = No	0 = No	0 = No	0 = No	0 = No
1 = Yes	1 = Yes	1 = Yes	1 = Yes	1 = Yes	1 = Yes	1 = Yes	1 = Yes

INTERRUPT MASK REGISTER (IMR)

Input Port Change $\overline{IRQ}$	Delta Break B $\overline{IRQ}$	RxRDYB/ FFULLB $\overline{IRQ}$	TxRDYB $\overline{IRQ}$	Counter/ Timer Ready $\overline{IRQ}$	Delta Break A $\overline{IRQ}$	RxRDYA/ FFULLA $\overline{IRQ}$	TxRDYA $\overline{IRQ}$
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 = Masked	0 = Masked	0 = Masked	0 = Masked	0 = Masked	0 = Masked	0 = Masked	0 = Masked
1 = Pass	1 = Pass	1 = Pass	1 = Pass	1 = Pass	1 = Pass	1 = Pass	1 = Pass

Table 6. Register Bit Formats (Concluded)

COUNTER/TIMER UPPER REGISTER (CTUR)

C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

COUNTER/TIMER LOWER REGISTER (CTLR)

C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

INTERRUPT VECTOR REGISTER (IVR)

IVR[7]	IVR[6]	IVR[5]	IVR[4]	IVR[3]	IVR[2]	IVR[1]	IVR[0]
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

INPUT PORT

*	**	IP5	IP4	IP3	IP2	IP1	IP0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

*Bit 7 has no external pin. Upon reading the input port, bit 7 will always be read as a one.
**Bit 6 has no external pin. Upon reading the input port, bit 6 will reflect the current logic level of $\overline{\text{IACK}}$.

OUTPUT PORT

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Bit 7 / $\overline{\text{OPR[7]}}$	Bit 6 / $\overline{\text{OPR[6]}}$	Bit 5 / $\overline{\text{OPR[5]}}$	Bit 4 / $\overline{\text{OPR[4]}}$	Bit 3 / $\overline{\text{OPR[3]}}$	Bit 2 / $\overline{\text{OPR[2]}}$	Bit 1 / $\overline{\text{OPR[1]}}$	Bit 0 / $\overline{\text{OPR[0]}}$

ELECTRICAL SPECIFICATIONS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +6.0	V
Input Voltage	V_{in}	−0.5 to +6.0	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

THERMAL CHARACTERISTICS

Characteristic	Value		Rating
	θ_{JA}	θ_{JC}	
Thermal Resistance (Still Air)			°C/W
Ceramic, Type L	50	25*	
Plastic, Type P			
Cu Lead Frame	50	25*	
A42 Lead Frame	100	50*	
PLCC, Type FN	TBD	TBD	

*Estimated

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POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

where:

T_A = Ambient Temperature, °C
θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
P_D = $P_{INT} + P_{I/O}$
P_{INT} = $I_{CC} \times V_{CC}$, Watts – Chip Internal Power
$P_{I/O}$ = Power Dissipation on Input and Output Pins – User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

The following is an approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected):

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \cdot (T_A + 273°C) + \theta_{JA} \cdot P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JA} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case) surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}). These terms are related by the equation:

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} aproximately equals θ_{JC}. Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

Values for thermal resistance presented in this document, unless estimated, were derived using the procedure described in Motorola Reliability Report 7843, "Thermal Resistance Measurement Method for MC68XX Microcomponent Devices," and are provided for design purposes only. Thermal measurements are complex and dependent on procedure and setup. User-derived values for thermal resistance may differ.

DC ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5.0 V ±5%)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage, Except X1/CLK	V_{IH}	2.0	—	—	V
Input High Voltage, X1/CLK	V_{IH}	4.0	—	—	V
Input Low Voltage	V_{IL}	—	—	0.8	V
Output High Voltage, Except Open-Collector Outputs (I_{OH} = −400 μA)	V_{OH}	2.4	—	—	V
Output Low Voltage (I_{OL} = 2.4 mA)	V_{OL}	—	—	0.4	V
Input Leakage Current (V_{in} = 0 to V_{CC})	I_{IL}	−10	—	10	μA
Data Bus Hi-Z Leakage Current (V_{out} = 0 to V_{CC})	I_{LL}	−10	—	10	μA
Open-Collector Output Leakage Current (V_{out} = 0 to V_{CC})	I_{OC}	−10	—	10	μA
Power Supply Current	I_{CC}	—	—	150	mA
Capacitance (V_{in} = 5 V, T_A = 25°C, f = 1 MHz)	C_{in}	—	—	15	pF
Load Capacitance Interrupt Outputs All Other Outputs	C_L	—	—	 50 150	pF
X1/CLK Low Input Current V_{in} = 0, X2 Grounded V_{in} = 0, X2 Floated	I_{X1L}	 −4.0 −3.0	 −2.0 −1.5	 0 0	mA
X1/CLK High Input Current V_{in} = V_{CC}, X2 Grounded V_{in} = V_{CC}, X2 Floated	I_{X1H}	 −1.0 0	 0.2 3.5	 1.0 10.0	mA
X2 Low Input Current V_{in} = 0, X1/CLK Floated	I_{X2L}	−100	−30	0	μA
X2 High Input Current V_{in} = V_{CC}, X1/CLK Floated	I_{X2H}	0	30	100	μA

AC ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5.0 V ±5%)

Characteristic	Symbol	Min	Max	Unit
X1/CLK Frequency (see Note 2)	f_{CLK}	2.0	4.0	MHz
Counter/Timer Clock Frequency	f_{CTC}	0	4.0	MHz
Receiver Clock Frequency (RxC) 16X Clock 1X Clock	f_{Rx}	 0 0	 2.0 1.0	MHz
Transmitter Clock Frequency (TxC) 16X Clock 1X Clock	f_{Tx}	 0 0	 2.0 1.0	MHz

NOTES:
1. All voltage measurements are referenced to GND. For testing, all input signals except X1/CLK swing between 0.4 V and 2.4 V with a maximum transition time of 20 ns. For X1/CLK, this swing is between 0.4 V and 4.4 V. All time measurements are referenced at input and output voltages of 0.8 V and 2.0 V, as appropriate. Test conditions for outputs C_L = 150 pF, R_L = 750 Ω to V_{CC}.
2. To use the standard baud rates selected by the clock select register given in Table 6, the X1/CLK frequency should be set to 3.6864 MHz or a 3.6864-MHz crystal should be connected across pins X1/CLK and X2.

AC ELECTRICAL CHARACTERISTICS—$\overline{\text{RESET}}$ TIMING (see Figure 3)

Characteristic	Symbol	Min	Max	Unit
$\overline{\text{RESET}}$ Pulse Width	t_{RES}	1.0	—	μs

NOTE: All voltage measurements are referenced to GND. For testing, all input signals swing between 0.4 V and 2.4 V with a maximum transition time of 20 ns. All time measurements are referenced at input and output voltages of 0.8 V and 2.0 V, as appropriate. Test conditions for noninterrupt outputs: $C_L = 150$ pF, $R_L = 750\ \Omega$ to V_{CC}. Test conditions for interrupt outputs: $C_L = 50$ pF, $R_L = 27\ k\Omega$ to V_{CC}.

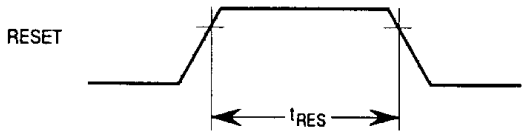


Figure 3. $\overline{\text{RESET}}$ Timing

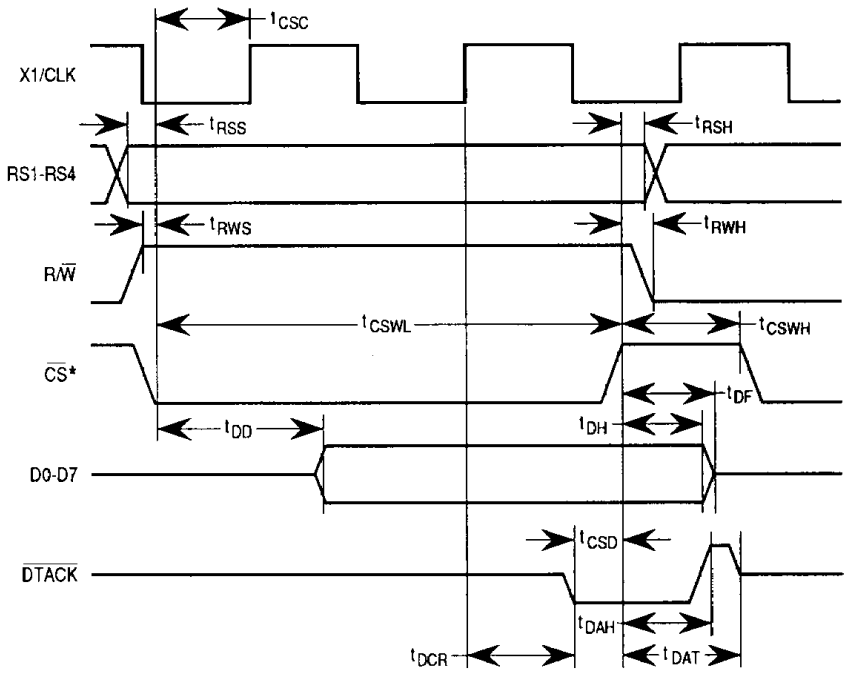
AC ELECTRICAL CHARACTERISTICS — READ CYCLE BUS TIMING

(see Figure 4)

Characteristic	Symbol	Min	Max	Unit
$\overline{\text{CS}}$ Setup Time to X1/CLK High (see Note 2)	t_{CSC}	90	—	ns
RS1–RS4 Setup Time to $\overline{\text{CS}}$ Asserted	t_{RSS}	10	—	ns
R/$\overline{\text{W}}$ Setup Time to $\overline{\text{CS}}$ Asserted	t_{RWS}	0	—	ns
$\overline{\text{CS}}$ Pulse Width Asserted (see Note 3)	t_{CSWL}	205	—	ns
Data Valid from $\overline{\text{CS}}$ Asserted	t_{DD}	—	175	ns
$\overline{\text{DTACK}}$ Asserted from X1/CLK High	t_{DCR}	—	125	ns
$\overline{\text{CS}}$ Negated from $\overline{\text{DTACK}}$ Asserted (see Note 3)	t_{CSD}	20	—	ns
RS1–RS4 Hold Time from $\overline{\text{CS}}$ Negated	t_{RSH}	0	—	ns
R/$\overline{\text{W}}$ Hold Time from $\overline{\text{CS}}$ Negated	t_{RWH}	0	—	ns
Data Hold Time from $\overline{\text{CS}}$ Negated	t_{DH}	0	—	ns
Data Bus Floating from $\overline{\text{CS}}$ Negated	t_{DF}	—	100	ns
$\overline{\text{DTACK}}$ Negated from $\overline{\text{CS}}$ Negated	t_{DAH}	—	100	ns
$\overline{\text{DTACK}}$ Hi-Z from $\overline{\text{CS}}$ Negated	t_{DAT}	—	125	ns
$\overline{\text{CS}}$ Pulse Width Negated	t_{CSWH}	90	—	ns

NOTES:

1. All voltage measurements are referenced to GND. For testing, all input signals except X1/CLK swing between 0.4 V and 2.4 V with a maximum transition time of 20 ns. For X1/CLK, this swing is between 0.4 V and 4.4 V. All time measurements are referenced at input and output voltages of 0.8 V and 2.0 V, as appropriate. Test conditions for noninterrupt outputs: $C_L = 150$ pF, $R_L = 750\ \Omega$ to V_{CC}. Test conditions for interrupt outputs: $C_L = 50$ pF, $R_L = 27\ k\Omega$ to V_{CC}.
2. This specification is made only to ensure $\overline{\text{DTACK}}$ is asserted with respect to the rising edge of X1/CLK as shown in Figure 4, not to guarantee operation of the part. If the setup time is violated, $\overline{\text{DTACK}}$ may be asserted as shown or may be asserted one clock cycle later.
3. The t_{CSD} specification is made only to ensure that $\overline{\text{DTACK}}$ will be asserted. If $\overline{\text{CS}}$ is negated before $\overline{\text{DTACK}}$ is asserted, $\overline{\text{DTACK}}$ may not be asserted.



* CS and IACK should not be asserted simultaneously.

Figure 4. Read Cycle Bus Timing

AC ELECTRICAL CHARACTERISTICS — WRITE CYCLE BUS TIMING

(see Figure 5)

Characteristic	Symbol	Min	Max	Unit
$\overline{CS}$ Setup Time to X1/CLK High (see Note 2)	t_{CSC}	90	—	ns
RS1–RS4 Setup Time to $\overline{CS}$ Asserted	t_{RSS}	10	—	ns
R/$\overline{W}$ Setup Time to $\overline{CS}$ Asserted	t_{RWS}	0	—	ns
$\overline{CS}$ Pulse Width Asserted (see Notes 3 and 4)	t_{CSWL}	205	—	ns
Data Setup Time to X1/CLK High (see Note 4)	t_{DS}	100	—	ns
Data Setup Time to $\overline{CS}$ Negated (see Note 4)	t_{DSCS}	100	—	ns
$\overline{DTACK}$ Asserted from X1/CLK High	t_{DCW}	—	125	ns
$\overline{CS}$ Negated from $\overline{DTACK}$ Asserted (see Note 3)	t_{CSD}	20	—	ns
RS1–RS4 Hold Time from $\overline{CS}$ Negated	t_{RSH}	0	—	ns
R/$\overline{W}$ Hold Time from $\overline{CS}$ Negated	t_{RWH}	0	—	ns
Data Hold Time from $\overline{CS}$ Negated	t_{DH}	0	—	ns
$\overline{DTACK}$ Negated from $\overline{CS}$ Negated	t_{DAH}	—	100	ns
$\overline{DTACK}$ Hi-Z from $\overline{CS}$ Negated	t_{DAT}	—	125	ns
$\overline{CS}$ Pulse Width Negated (see Note 5)	t_{CSWH}	90	—	ns

NOTES:

1. All voltage measurements are referenced to GND. For testing, all input signals except X1/CLK swing between 0.4 V and 2.4 V with a maximum transition time of 20 ns. For X1/CLK, this swing is between 0.4 V and 4.4 V. All time measurements are referenced at input and output voltages of 0.8 V and 2.0 V, as appropriate. Test conditions for noninterrupt outputs: $C_L = 150$ pF, $R_L = 750\ \Omega$ to V_{CC}. Test conditions for interrupt outputs: $C_L = 50$ pF, $R_L = 27\ k\Omega$ to V_{CC}.
2. This specification is made only to ensure $\overline{DTACK}$ is asserted with respect to the rising edge of X1/CLK as shown in Figure 4, not to guarantee operation of the part. If the setup time is violated, $\overline{DTACK}$ may be asserted as shown or maybe asserted one clock cycle later.
3. The t_{CSD} specification is made only to ensure that $\overline{DTACK}$ will be asserted. If $\overline{CS}$ is negated before $\overline{DTACK}$ is asserted, $\overline{DTACK}$ may not be asserted.
4. During write cycles, data is latched on either the asserting edge of $\overline{DTACK}$ or the negating edge of $\overline{CS}$, whichever occurs first. If $\overline{CS}$ is negated within one clock cycle after $\overline{CS}$ has been recognized (i.e., first rising edge of X1/CLK where $\overline{CS}$ is asserted), then $\overline{DTACK}$ may not be generated. In this case, data will be latched on the negating edge of $\overline{CS}$. Thus, t_{DS} can be ignored, but t_{DSCS} must be observed.
5. Consecutive write operations to the same command register (CRA or CRB) require at least three transitions of X1/CLK between write cycles. Typically, a processor is incapable of accessing the same command register a second time prior to three transitions on the X1/CLK pin.

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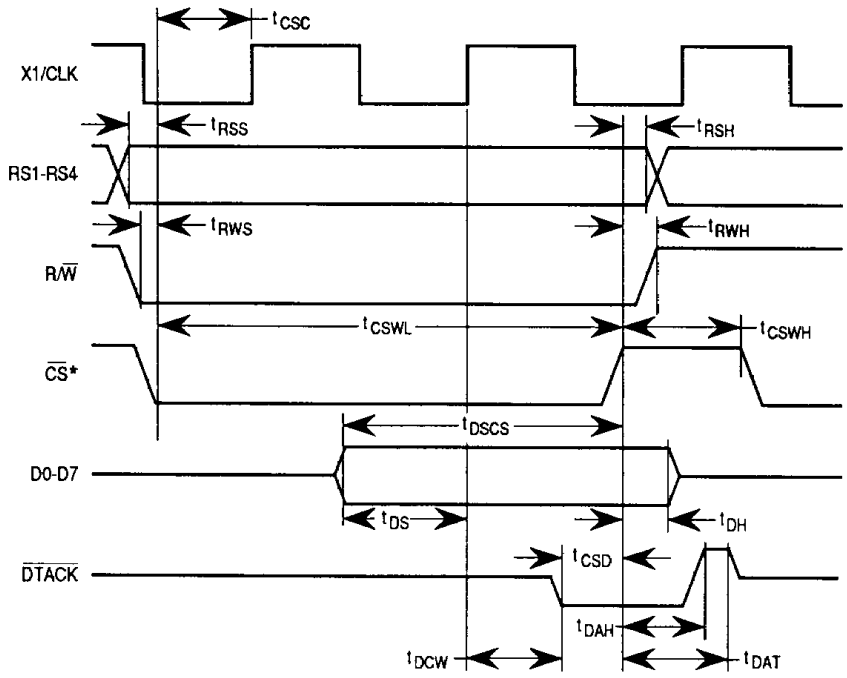


* $\overline{CS}$ and $\overline{IACK}$ should not be asserted simultaneously.

Figure 5. Write Cycle Bus Timing

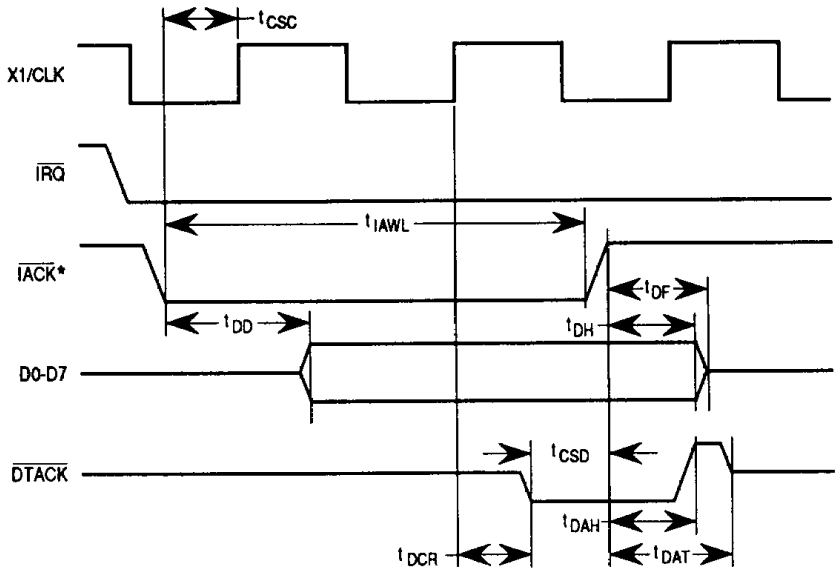
AC ELECTRICAL CHARACTERISTICS — INTERRUPT CYCLE BUS TIMING* (see Figure 6)

Characteristic	Symbol	Min	Max	Unit
$\overline{IACK}$ Setup Time to X1/CLK High (see Note 2)	t_{CSC}	90	—	ns
$\overline{IACK}$ Pulse Width Asserted (see Note 3)	t_{IAWL}	205	—	ns
Data Valid from $\overline{IACK}$ Asserted	t_{DD}	—	175	ns
$\overline{DTACK}$ Asserted from X1/CLK High	t_{DCR}	—	125	ns
$\overline{IACK}$ Negated from $\overline{DTACK}$ Asserted (see Note 3)	t_{CSD}	0	—	ns
Data Hold Time from $\overline{IACK}$ Negated	t_{DH}	0	—	ns
Data Bus Floating from $\overline{IACK}$ Negated	t_{DF}	—	100	ns
$\overline{DTACK}$ Negated from $\overline{IACK}$ Negated	t_{DAH}	—	100	ns
$\overline{DTACK}$ Hi-Z from $\overline{IACK}$ Negated	t_{DAT}	—	125	ns

*During interrupt acknowledge cycles, the status of R/$\overline{W}$ is ignored.

NOTES:

1. All voltage measurements are referenced to GND. For testing, all input signals except X1/CLK swing between 0.4 V and 2.4 V with a maximum transition time of 20 ns. For X1/CLK, this swing is between 0.4 V and 4.4 V. All time measurements are referenced at input and output voltages of 0.8 V and 2.0 V, as appropriate. Test conditions for noninterrupt outputs: $C_L = 150$ pF, $R_L = 750\ \Omega$ to V_{CC}. Test conditions for interrupt outputs: $C_L = 50$ pF, $R_L = 27\ k\Omega$ to V_{CC}.
2. This specification is made only to ensure $\overline{DTACK}$ is asserted with respect to the rising edge of X1/CLK as shown in Figure 4, not to guarantee operation of the part. If the setup time is violated, $\overline{DTACK}$ may be asserted as shown or may be asserted one clock cycle later.
3. The t_{CSD} specification is made only to ensure that $\overline{DTACK}$ will be asserted. If $\overline{CS}$ is negated before $\overline{DTACK}$ is asserted, $\overline{DTACK}$ may not be asserted.



* $\overline{CS}$ and $\overline{IACK}$ should not be asserted simultaneously.

Figure 6. Interrupt Cycle Bus Timing

AC ELECTRICAL CHARACTERISTICS — PORT TIMING (see Figure 7)

Characteristic	Symbol	Min	Max	Unit
Port Input Setup Time to $\overline{CS}$ Asserted	t_{PS}	0	—	ns
Port Input Hold Time from $\overline{CS}$ Negated	t_{PH}	0	—	ns
Port Output Valid from $\overline{CS}$ Negated	t_{PD}	—	400	ns

NOTE: All voltage measurements are referenced to GND. For testing, all signals except X1/CLK swing between 0.4 V and 2.4 V with a maximum transition time of 20 ns. For X1/CLK, this swing is between 0.4 V and 4.4 V. All time measurements are referenced at input and output voltages of 0.8 V and 2.0 V, as appropriate. Test conditions for noninterrupt outputs: $C_L = 150$ pF, $R_L = 750\ \Omega$ to V_{CC}. Test conditions for interrupt outputs: $C_L = 50$ pF, $R_L = 27\ k\Omega$ to V_{CC}.

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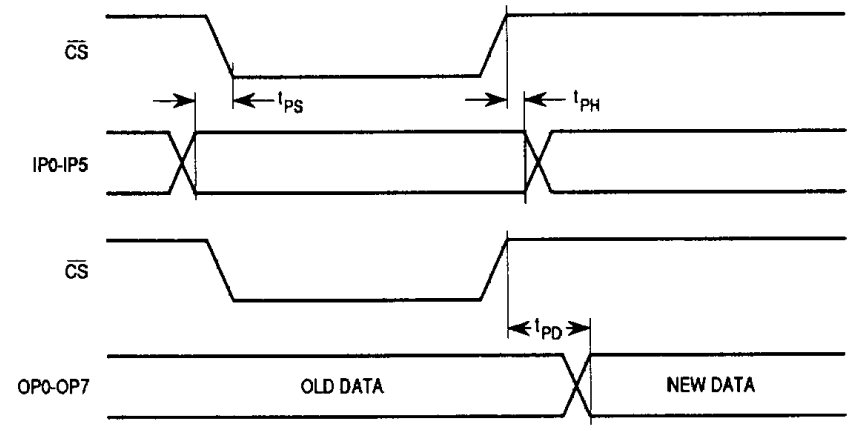


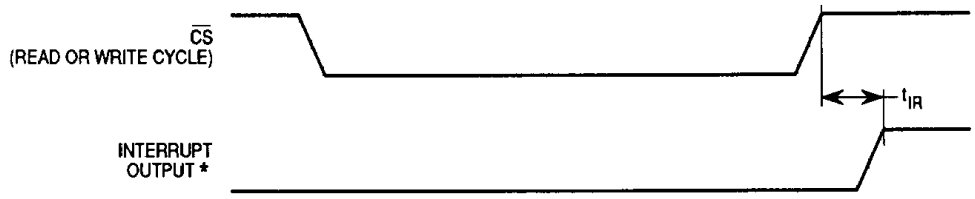
Figure 7. Port Timing

AC ELECTRICAL CHARACTERISTICS—INTERRUPT RESET TIMING

(see Figure 8)

Characteristic	Symbol	Min	Max	Unit
$\overline{IRQ}$ Negated or OP3–OP7 High from $\overline{CS}$ Negated When Used as Interrupts from:	t_{IR}			ns
Read RB (RxRDY/FFULL Interrupt)		—	300	
Write TB (TxRDY Interrupt)		—	300	
Reset Command (Delta Break Interrupt)		—	300	
Stop C/T Command (Counter Interrupt)		—	300	
Read IPCR (Input Port Change Interrupt)		—	300	
Write IMR (Clear of Interrupt Mask Bit)		—	300	

NOTE: All voltage measurements are referenced to GND. For testing, all input signals except X1/CLK swing between 0.4 V and 2.4 V with a maximum transition time of 20 ns. For X1/CLK, this swing is between 0.4 V and 4.4 V. All time measurements are referenced at input and output voltages of 0.8 V and 2.0 V, as appropriate. Test conditions for noninterrupt outputs: $C_L = 150$ pF, $R_L = 750\ \Omega$ to V_{CC}. Test conditions for interrupt outputs: $C_L = 50$ pF, $R_L = 27\ k\Omega$ to V_{CC}.



* $\overline{IRQ}$ or OP3-OP7 when used as interrupt outputs.

Figure 8. Interrupt Reset Timing

AC ELECTRICAL CHARACTERISTICS — CLOCK TIMING (see Figure 9)

Characteristic	Symbol	Min	Max	Unit
X1/CLK High or Low Time	t_{CLK}	100	—	ns
Counter/Timer Clock High or Low Time	t_{CTC}	100	—	ns
Receive Clock (RxC) High or Low Time	t_{Rx}	220	—	ns
Transmit Clock (TxC) High or Low Time	t_{Tx}	220	—	ns
Clock Rise Time	t_r	—	20	ns
Clock Fall Time	t_f	—	20	ns

NOTE: All voltage measurements are referenced to GND. For testing, all signals except X1/CLK swing between 0.4 V and 2.4 V with a maximum transition time of 20 ns. For X1/CLK, this swing is between 0.4 V and 4.4 V. All time measurements are referenced at input and output voltages of 0.8 V and 2.0 V, as appropriate. Test conditions for noninterrupt outputs: $C_L = 150$ pF, $R_L = 750\ \Omega$ to V_{CC}. Test conditions for interrupt outputs: $C_L = 50$ pF, $R_L = 27\ k\Omega$ to V_{CC}.

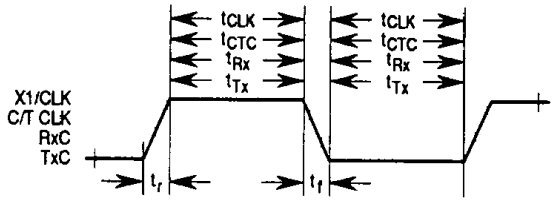


Figure 9. Clock Timing

AC ELECTRICAL CHARACTERISTICS — TRANSMITTER TIMING

(see Figure 10)

Characteristic	Symbol	Min	Max	Unit
TxD Output Valid from TxC Low	t_{TxD}	—	350	ns
TxC Low to TxD Output Valid	t_{TCS}	—	150	ns

NOTE: All voltage measurements are referenced to GND. For testing, all signals except X1/CLK swing between 0.4 V and 2.4 V with a maximum transition time of 20 ns. For X1/CLK, this swing is between 0.4 V and 4.4 V. All time measurements are referenced at input and output voltages of 0.8 V and 2.0 V, as appropriate. Test conditions for noninterrupt outputs: $C_L = 150$ pF, $R_L = 750\ \Omega$ to V_{CC}. Test conditions for interrupt outputs: $C_L = 50$ pF, $R_L = 27\ k\Omega$ to V_{CC}.

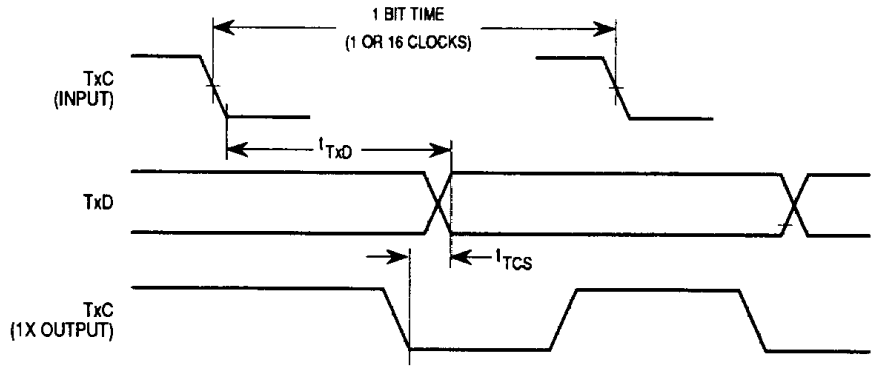


Figure 10. Transmitter Timing

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AC ELECTRICAL CHARACTERISTICS — RECEIVER TIMING (see Figure 11)

Characteristics	Symbol	Min	Max	Unit
RxD Data Setup Time to RxC High	t_{RxS}	240	—	ns
RxD Data Hold Time from RxC High	t_{RxH}	200	—	ns

NOTE: All voltage measurements are referenced to GND. For testing, all signals except X1/CLK swing between 0.4 V and 2.4 V with a maximum transition time of 20 ns. For X1/CLK, this swing is between 0.4 V and 4.4 V. All time measurements are referenced at input and output voltages of 0.8 V and 2.0 V, as appropriate. Test conditions for noninterrupt outputs: $C_L = 150$ pF, $R_L = 750\ \Omega$ to V_{CC}. Test conditions for interrupt outputs: $C_L = 50$ pF, $R_L = 27\ k\Omega$ to V_{CC}.

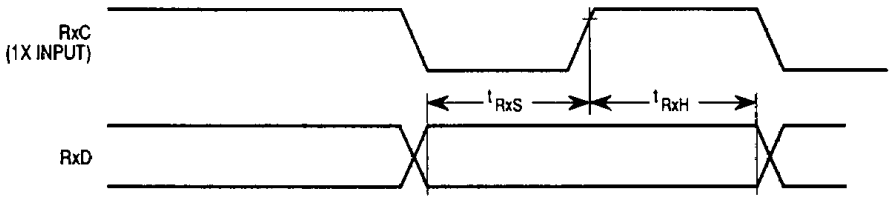

Figure 11. Receiver Timing

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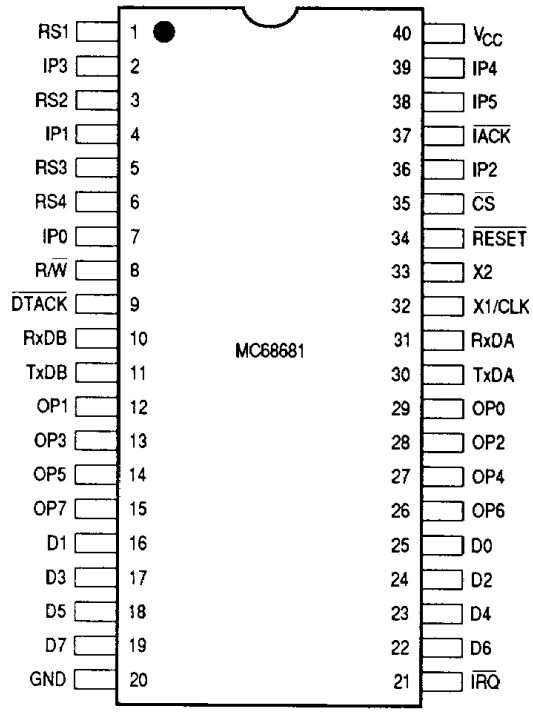
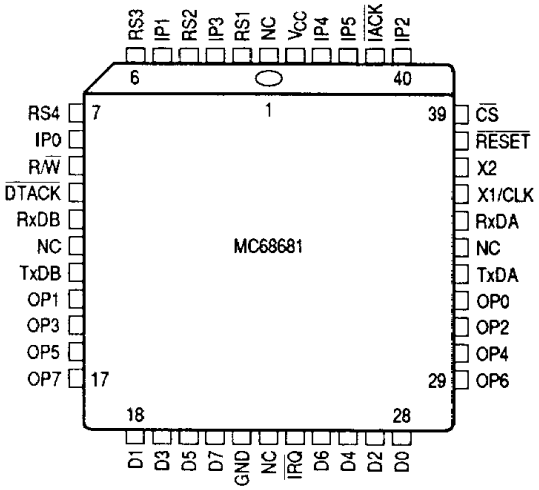
PIN ASSIGNMENTS

40-LEAD DUAL-IN-LINE PACKAGE



44-LEAD PLASTIC LEADED CHIP CARRIER



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